

Applicant : Alpesh B. Oza et al.
Serial No. : 10/816,801
Filed : April 1, 2004
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Attorney Docket: 10559-923001 / P18646

Amendments to the Drawings:

The attached replacement sheet of drawing includes changes to FIG. 3 and replaces the original sheet including FIG. 3.

In FIG. 3, the microengine labeled "ME07" in ME cluster 1 has been changed to "ME17".

Attachments following last page of this Amendment:

Replacement Sheet (1 pages)

REMARKS

Applicant thanks the Examiner for the telephone interview on November 15, 2006. Applicant's representative and the Examiner discussed the claims, the specification, and MPEP sections 2165 to 2165.03, and concluded that the best mode requirement has been satisfied. Also discussed were reasons why the other rejections under 35 U.S.C. 112, 101, and 102 are improper, as set forth below.

The examiner rejected Claims 1-14, 18-20 and 28-30 under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The examiner stated in part:

"It is noted that in the specification, there is no disclosure of or suggestion that the disclosed invention could be implemented by computer software as claimed in claims 1-14, 18-20 and 28-30."

Original claim 1 is directed to an apparatus including a write data module ... and a read data module ... not to computer software per se whereas claim 18 is directed to a network router. The claimed "write data module" and "read data module" recited in claims 1-14 and 18-20 may be implemented either by computer software or hardware at the discretion of one of ordinary skill. FIG. 2 and page 3, line 3 to page 6, line 9 of Applicant's specification provide a description of how the write data module 120 and the read data module 122 operate. FIGS. 4 and 5 and page 8, lines 3-31 of Applicant's specification provide a description of a process 230 for writing data using the write data module 120, and a process 250 for reading data using the read data module 122. Moreover, the operations recited in claims 28-30 are described in FIGS. 4 and 5 and page 8, lines 3-31.

Thus, Applicant's specification has described the claimed invention of Claims 1-14, 18-20, and 28-30 in sufficient detail that one skilled in the art can reasonably conclude that the inventor had possession of the claimed invention.

The examiner rejected Claims 1-14, 18-20 and 28-30 under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The examiner stated in part:

... The specification lacks any description of the claimed software modules or machine accessible medium.

Claims 1-14, 18-20 and 28-30 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. Software instructions critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

Claims 1-14 and 18-20 recite computer program modules which require instructions on a computer readable medium to be able to be implemented by an apparatus, however these instructions are not disclosed or recited in the claims.

Claims 28-30 recite a "machine-accessible medium" that is able to cause a "machine" to perform the recited operations, but a medium, in order to cause a computer (or machine) to carry out operations would need to have computer (machine) instructions contained therein, which are lacking in claims 28-30 and are not disclosed in the specification.

Applicant's specification provides a clear description of how the write data module and the read data module operate, as well as the processes for using the read and write data modules to read and write data. The write data module and the read data module recited in Claims 1-14 and 18-20 can be hardware or software modules. Applicant did not provide detailed circuit diagrams for implementing hardware read and write data modules or a listing of program code for implementing software read and write data modules because a person skilled in the art would know how to implement the software and/or hardware modules after reading Applicant's specification.

A patent need not teach, and preferably omits, what is well known in the art. *In re Buchner*, 929 F.2d 660, 661, 18 USPQ2d 1331, 1332 (Fed. Cir. 1991); *Hybritech, Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 1384, 231 USPQ 81, 94 (Fed. Cir. 1986), cert. denied, 480 U.S. 947 (1987); and *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1463, 221 USPQ 481, 489 (Fed. Cir. 1984). Applicant submits that the detailed description of the functions to be performed by the claimed invention sufficiently enable one of ordinary skill to practice the claimed invention. Indeed, the absence of detailed circuit diagrams and specific computer instructions serves to help define and teach the essence of the claimed invention whereas in contrast inclusion of such detailed circuit diagrams and computer instructions would serve to obfuscate the invention. Accordingly, the detailed description in Applicant's specification enables any person skilled in the art to make and use the invention without undue experimentation. Thus, the enablement requirement has been satisfied.

The examiner rejected claims 28-30 under 35 U.S.C. 112, second paragraph as being incomplete. The examiner stated:

Claims 28-30 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: the computer instructions contained on the recited machine accessible medium, which would cause a machine to carry out the recited operations.

Claim 28 has been amended to call A machine-accessible medium having instructions stored thereon, the instructions when executed cause a machine to ...

The examiner rejected Claims 15-17 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The examiner stated:

Claims 15-17 provide for the use of a memory, but, since the claim does not set forth any steps involved in the method/process, it is unclear what method/process applicant is intending to encompass. A claim is indefinite where it merely recites a use without any active, positive steps delimiting how this use is actually practiced.

Claim 15 is directed to an apparatus that includes a memory. Claim 15 is not directed to a method process.

The examiner rejected Claims 15-17 under 35 U.S.C. 101 as being directed to non-statutory subject matter. The examiner stated:

Claims 15-17 are rejected under 35 U.S.C. 101 because the claimed recitation of a use for a memory, without setting forth any steps involved in the process, results in an improper definition of a process, i.e., results in a claim which is not a proper process claim under 35 U.S.C. 101. See for example Ex pane Dunki, 153 USPQ 678 (Bd. App. 1967) and Clinical Products, Ltd. v. Brenner, 255 F. Supp. 131, 149 USPQ 475 (D.D.C. 1966). It is noted that the only apparatus recited in these claims is a memory, which is well known in the prior art, which is used for storing the recited data structures.

Claim 15 is an apparatus claim that includes a memory, an article of manufacture. Claim 15 is not a process claim.

Moreover, Claim 15 does not claim nonfunctional descriptive materials such as music, literary works and a compilation or mere arrangement of data. Rather, Claim 15 claims functional elements, e.g., a user data unit and an error correction code unit stored in a memory that enables, e.g., a network processor to function more efficiently.

Assuming the novelty of the claimed user data unit and an error correction code unit, as discussed below, the memory becomes a new article of manufacture in which the novel elements are entitled to patentable weight that must be given consideration by the examiner. See *In re Lowry*, 32 F.3d 1579, 32 USPQ2d 1031 (Fed. Cir. 1994) in which the Federal Circuit set forth guidelines to be applied by the patent office in evaluating claims directed to data structures

The Federal Circuit noted that: "Lowry disclosed a data structure accessible by many different application programs. Lowry's data structure was based upon the 'Attributive data model.' The Attributive data model represents complex information in terms of attributes and relationships between attributes." *Lowry* F.3d at 1582. After acknowledging that the Board of Patent Appeals and Interferences had reversed the examiner's rejection of Lowry's data structure claims under 35 U.S.C. 101 because Lowry recited a memory, an article of manufacture and a class of invention specifically prescribed by 35 U.S.C. 101, the court turned to the printed matter rejection of those claims that was furnished by the Board. In reversing the Board, the Federal Circuit stated:

More than mere abstraction, the data structures are specific electrical or magnetic *1584 structural elements in a memory. According to Lowry, the data structures provide tangible benefits: data stored in accordance with the claimed data structures are more easily accessed, stored, and erased. Lowry further notes that, unlike prior art data structures, Lowry's data structures simultaneously represent complex data accurately and enable powerful nested operations. In short, Lowry's data structures are physical entities that provide increased efficiency in computer operation. They are not analogous to printed matter. The Board is not at liberty to ignore such limitations.

In accord is *In re Warmerdam*, 33 F.3d, 1354 31 USPQ2d 1754 (Fed. Cir.1994) where the Federal Circuit found claim 5 directed to "a machine, and is clearly patentable subject matter." 33 F.3d at 1360-61, 31 USPQ2d at 1759. In contrast the Federal Circuit found claims 1-

4 and 6 reciting “steps [that] describe nothing more than the manipulation of basic mathematical constructs, the paradigmatic “abstract idea.”¹

Unlike the situation in claims 1-4 and 6 in *Warmerdam* instant claim 15 calls for a memory storing a user data unit in a first memory region and an error correction code unit at a second memory region, the error correction code unit used to correct one or more bits of error in the user data unit if error occurs, the second memory region being in a different address location from the first memory region so that the user data can be read independently of reading the error correction code unit. Thus, claim 15 by calling for a memory recites statutory subject matter under 35 U.S.C. 101. As in *Lowry*, these claims are “More than mere abstraction, the data structures are specific electrical or magnetic structural elements in a memory.” *Lowry*, 32 F.3d at 1583-1584.

Claims 1-14 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 1-14 recite a computer program per se. Data structures (such as the “modules” recited in applicants’ claims 1-14) not claimed as embodied in computer-readable media are descriptive material per se and are not statutory because they are not capable of causing functional change in the computer. See, e.g., *Warmerdam*, 33 F.3d at 1361, 31 USPQ2d at 1760 (claim to a data structure per se held nonstatutory). Such claimed data structures do not define any structural and functional interrelationships between the data structure and other claimed aspects of the invention which permit the data structure’s functionality to be realized. In contrast, a claimed computer-readable medium encoded with a data structure defines structural and functional interrelationships between the data structure and the computer software and hardware components which permit the data structure’s functionality to be realized, and is thus statutory.

Claims 1-8 directed to an apparatus that includes a write data module and a read data module. Claims 9-14 are directed to an apparatus that includes a write data module. The read and write data modules in Claims 1-8 and 9-14 can be either software or hardware modules. Thus, Claims 1-14 do not recite a computer program per se.

¹ “Nonfunctional descriptive material” includes but is not limited to music, literary works and a compilation or mere arrangement of data. Both types of “descriptive material” are nonstatutory when claimed as descriptive material per se. *Warmerdam*, 33 F.3d at 1360, 31 USPQ2d at 1759. When functional descriptive material is recorded on some computer-readable medium it becomes structurally and functionally interrelated to the medium and will be statutory in most cases since use of technology permits the function of the descriptive material to be realized.

The examiner rejected Claims 1-10, 12-17 and 21-30 under 35 U.S.C. 102(b) as being fully anticipated by Malakapalli et al. (6,467,060). The examiner stated:

Claims 1-10, 12-17 and 21-30 are rejected under 35 U.S.C. 102(b) as being fully anticipated by Malakapalli et al. (6,467,060) which teaches a write data module to write user data, parity information, and error correction information in a memory ("an error correction code (ECC) and a CRC are generated from a sector of data, and the IOEDC, ECC and CRC are stored on disc", abstract of Malakapalli et al.) and a read data module to read the user data and parity information, determine whether there is error in the user data based on the parity information, and read error correction information if there is error as determined based on the parity information "Subsequently, a second CRC seeded with the PBA from the read request is generated from the sector of data 720 and the second CRC and original CRC are compared for equality to verify data integrity 730. If the comparison indicates equality, processing continues, however, if the comparison does not indicate equality, then an attempt in correcting the error using the ECC is made 733" (Column 10, line 64 to column 11, line 3 of Malakapalli et al.) where the memory has addresses (see the paragraph starting at the bottom of column 5 of Malakapalli et al.) which is implemented by computer program ("The present invention also can be implemented as a computer readable program storage device which tangibly embodies a program of instructions executable by a computer system to perform the present mass-storage device error detection and correction method" column 2, lines 55-59).

Claims 1-8, 21-23, and 28-30

Malakapalli does not disclose and would not have suggested "a read data module to read the user data and parity information, determine whether there is error in the user data based on the parity information, and read error correction information if there is error as determined based on the parity information," as recited in claim 1. In claim 1, the error correction information is read after determining that there is error based on the parity information.

What Malakapalli describes is a mass storage device that reads a 512-byte sector of data 380, associated CRC 360, and ECC 365 under the direction of a read request (col. 7, lines 38-40, col. 9, lines 65-66, col. 10, lines 62-63, and col. 12, lines 63-64). Malakapalli does not disclose reading the ECC 365 separately from the data 380 and the CRC 360.

Claims 2-8 are patentable for at least the same reasons as those applied to claim 1. Moreover, these claims add additional distinctive features.

For example, claim 2 recites "wherein the read data module does not read the error correction information if there is no error." Claim 3 recites "the user data and error correction

information are stored in the memory such that the user data are read without reading the error correction information in the same read access to the memory.” Claim 7 recites “each address in the second set of addresses is associated with more than one unit of error correction information, each unit of error correction information being used to correct one or more errors in the user data associated with an address in the first set of addresses.” In Malakapalli, the error correction information is read along with the data.

Claim 21 is patentable for at least reasons similar to those applied to claim 1.

Claims 22-23 are patentable for at least the same reasons as those applied to claim 21.

Claim 28 is patentable for at least reasons similar to those applied to claim 1.

Claims 29-30 are patentable for at least the same reasons as those applied to claim 28.

Claims 9-14 and 24-27

Malakapalli does not disclose and would not have suggested “a write data module ... to store the error correction code unit in a second memory region of the memory so that the user data unit can be read independently of reading the error correction code unit,” as recited in claim 9.

Rather, Malakapalli discloses recording 30 bytes of ECC as overhead for each 512-byte sector of data (col. 7, lines 28-31). The ECC is read along with the 512-byte sector of data (col. 7, lines 38-40). Malakapalli does not disclose storing data and ECC in separate regions so that the data can be read independently of reading the ECC.

Claims 10-14 are patentable for at least the same reasons as those applied to claim 9. Moreover, these claims add additional distinctive features.

For example, claim 10 recites “the write data module writes a plurality of user data units into a corresponding plurality of addressable locations in the first region of memory and writes a like plurality of error correction code units into a second plurality of addressable locations in the second region of memory.” Claim 13 recites “a read data module to ... read the error correction code unit in the second memory region if there is an error.” Claim 14 recites “the read data module does not read the error correction code unit if there is no error in the user data unit.”

Malakapalli's mass storage device writes the ECC with each sector of data, and reads the error correction code along with each sector of data.

Claim 24 is patentable for at least reasons similar to those applied to claim 9.

Claims 25-27 are patentable for at least the same reasons as those applied to claim 24.

Claims 15-17

Malakapalli does not disclose and would not have suggested "a memory storing a user data unit in a first memory region and an error correction code unit at a second memory region, ..., the second memory region being in a different address location from the first memory region so that the user data can be read independently of reading the error correction code unit," as recited in claim 15.

Rather, Malakapalli disclose a mass storage device that stores ECC in the overhead of each sector of data (col. 7, lines 28-31). Malakapalli does not disclose a mass storage device that stores ECC in a second region that is different from a first region for storing data so that the data can be read independently of reading the ECC.

Claims 18-20 are rejected under 35 U.S.C. 102(b) as being fully anticipated by Geiger et al. (2003/0058873) which shows the combination of a network processor ("A network device, also referred to as the Compression Enhanced Network Processor (CENP)" abstract of Geiger et al.), a static random access memory ("a memory buffer (e.g., an SRAM memory buffer), and a system memory" abstract of Geiger et al.) and a memory controller ("a memory management unit", abstract of Geiger et al.)

Geiger does not disclose and would not have suggested "a memory controller ... having ... a read data module, ... the read data module to read the user data and parity information, determine whether there is error in the user data based on the parity information and read error correction information if there is error as determined based on the parity information," as recited in claim 18.

The Geiger reference does not discuss how parity information and error correction information are used, let alone a memory controller having a read data module that processes the parity information and the error correction information as recited in claim 18.

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Claims 19-20 are patentable for at least the same reasons as those applied to claim 18.

Any circumstance in which the applicant has addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner. Any circumstance in which the applicant has made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims. Any circumstance in which the applicant has amended or canceled a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

Please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: 11/30/2006

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